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S58	59	translat$3 with (key$4 identifier ID symbolic) with (target adj language) (	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 12:08
S60	8	S59 not S54	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 12:03
S59	32	S42 and S58	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 12:03
S53	45	translat$3 with (keyword identifier ID symbolic) with (target adj language)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 12:02
S57	8	(S44 S46 S48 S50 S52 S53) and S56	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 11:21
S56	116	(717/137).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 11:20
S41	866	(717/124,125,136).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 11:20
S55	18	S54 not S52	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 11:15
S54	24	S42 and S53	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 11:15

S52	12	translat$3 near3 (keyword identifier ID symbolic) with target adj language	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 11:15
S50	63	translat$3 near3 (keyword identifier ID) with target	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 11:05
S51	11	S42 and S50	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 10:51
S49	0	("2004/0205721").URPN.	USPAT	OR	ON	2004/11/19 10:50
S46	3875	translat$3 near3 (keyword identifier ID)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 10:50
S48	10	translat$3 near3 (keyword identifier ID) with symbolic	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 10:47
S47	87	S42 and S46	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 10:47
S45	99	S42 and S44	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 10:47
S44	4120	translat$3 near3 (keyword identifier ID symbolic)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 10:47
S37	417	translat$3 near3 script	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 10:46
S43	18	S42 and S37	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 10:45

S42	3286	S38 or S41	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 10:45
S40	0	717/124,125,136	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 10:44
S39	9	S37 and S38	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 10:44
S38	2430	(704/1-10).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 10:44
S36	146	translated near3 script	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/19 10:34

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transient current analysis for fault detection and localization
Swarup Bhunia, Kaushik Roy, Jaume Segura
June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: 📄 pdf(206.90 KB)   Additional Information: full citation, abstract, references, citings, index terms

Transient current (IDD) based testing has been often cited and investigated as an alternative and/or supplement to quiescent current (IDDQ) testing. While the potential of IDD testing for fault detection has been established, there is no known efficient method for fault diagnosis using IDD analysis. In this paper, we present a novel integrated method for fault detection and localization using wavelet transform based IDD waveform analysis. The time-frequency resolution property of wavelet transfo ...

Keywords: fault localization, transient current (IDD), wavelet transform

2 Technical papers: program analysis: Visualization of test information to assist fault   ◼
localization
James A. Jones, Mary Jean Harrold, John Stasko
May 2002 **Proceedings of the 24th International Conference on Software Engineering**

Full text available: 📄 pdf(1.45 MB)   Additional Information: full citation, abstract, references, citings, index terms

One of the most expensive and time-consuming components of the debugging process is locating the errors or faults. To locate faults, developers must identify statements involved in failures and select suspicious statements that might contain faults. This paper presents a new technique that uses visualization to assist with these tasks. The technique uses color to visually map the participation of each program statement in the outcome of the execution of the program with a test suite, consisting ...

3 Fault Localization Using Visualization of Test Information   ◼
May 2004 **Proceedings of the 26th International Conference on Software Engineering**

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Attempts to reduce the number of delivered faults in softwareare estimated to consume 50% to 80% of the developmentand maintenance effort [3]. Among the tasks requiredto reduce the number of delivered faults, debugging is oneof the most time-consuming [2, 12], and locating the errorsis the most dif.cult component of this debugging task (e.g.,[13]). Clearly, techniques that can reduce the time requiredto locate faults can have a signi.cant

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David Heller, Lisa Krenzelok, Julian Orr
June 2003 **Proceedings of the 2003 conference on Designing for user experiences**

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This case study focuses on the design process for a thin-client in a real world enterprise software environment, created for our own internal sales and marketing directives. This project became the basis of our biggest upgrade migration in four years. The project increased sales and earned our product industry awards, but was most successful for the paradigm shift in corporate culture; specifically, user experience has become a fundamental part of our development process, a challenge in most org ...

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2 **A pragmatic set operation and its implementation in C**
Tom Bennet
April 1992 **Proceedings of the 1992 ACM/SIGAPP Symposium on Applied computing: technological challenges of the 1990's**
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3 **Manufacturing applications: Manufacturing 1: simulation-based analysis of a complex printed circuit board testing process**
Jeffrey S. Smith, Yali Li, Jason Gjesvold
December 2002 **Proceedings of the 34th conference on Winter simulation: exploring new frontiers**
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This paper describes a simulation-based analysis of a printed circuit board (PCB) testing process. The PCBs are used in a defense application and the testing process is fairly complex. Boards are mounted on a test unit in batches and go through three thermal test cycles. As boards fail testing during the thermal cycling, operators can either replace the failed boards at fixed points during the cycling or can allow the test unit to complete the testing cycle before removing failed boards. The ...

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2 Annotated bibliography on internationalization and localization   ■
Emmanuel Uren
February 1997 **ACM SIGDOC Asterisk Journal of Computer Documentation**, Volume 21 Issue 1

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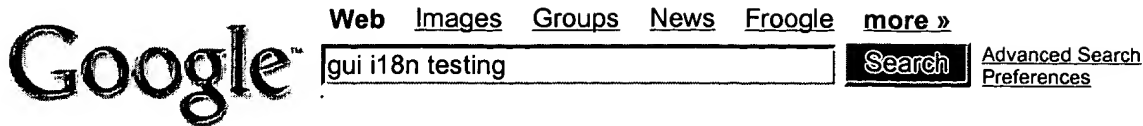March 1999 **Linux Journal**

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Memon, A.M.;
Computer , Volume: 35 , Issue: 8 , Aug. 2002
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2 **What test oracle should I use for effective GUI testing?**
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Daboczi, T.; Kollar, I.; Simon, G.; Megyeri, T.;
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